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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/787,499	02/26/2004	Shin Choi	CU-3609 RJS	4990

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EXAMINER	
CLARK, JASMINE JHIHAN B	
ART UNIT	**PAPER NUMBER**
2815	

DATE MAILED: 04/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/787,499	SHIN CHOI	
	Examiner	Art Unit	
	Jasmine J. Clark	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1, 3, 12/1* is/are rejected.

7)☒ Claim(s) *2, 4/1, 4/3, 5-11, and 12/11* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claim 1 is rejected under 35 U.S.C. 102(b) as being anticipated by Panchou et al. (US 6,218,214 B1).

Panchou teaches a device, comprising a circuit substrate 10 consisting of first, second and third areas which surround three sides of the multi-chip package; and at least two chips, for example 20 which are positioned within an internal space of the package defined by internal surfaces of the above three areas, wherein the semiconductor chips 34 are physically bonded and electrically connected to each other through conductive epoxy 32. (please see Fig. 2).

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 1, 3, and 12/1 are rejected under 35 U.S.C. 10(a) as being unpatentable over Nakatsuka (US 6,208,521 B1) in view of Panchou et al. (US 6,218,214 B1).

Nakatsuka shows in Fig. 7, a device package comprising a carrier member 1 which serves as a circuit substrate consisting of first, second and third areas which surround three sides (see top view without the right side) of the device package; and at least two semiconductor chips 8a and 8b which are positioned within an internal space of the device package defined by the internal surfaces of the above three areas, wherein the semiconductor chips 8a and 8b are physically bonded to each other. However, Nakatsuka fails to teach wherein the chips 8a and 8b are electrically connected to each other as the claimed invention. Panchou teaches bonding first and second semiconductor chips 34 with an adhesive such as a conductive epoxy 32 (see column 5, line 16) which is electrically connected to each other. Hence, it would have been obvious for Nakatsuka to practice using an adhesive such as the conductive epoxy as taught by Panchou, as is notoriously known in the art.

Concerning claim 3, wherein the semiconductor chips 8a and 8b comprises a plurality of chip pads (see connection parts 7) formed on the top surfaces of the semiconductor chips 8a and 8b and a plurality of chip bumps (also see connection parts 7) individually formed on each of the chip pads, respectively corresponding chip bumps and substrate pads that are physically bonded and electrically connected to each other, please see Figs. 1a, 1b, and/or Figs. 4a and 4b).

Concerning claim 12/1, the device according to claim 1, further comprising an encapsulant 9 filled in the internal space of the device package, please see Fig. 5 and see column 8, line 57.

3. Claims 2, 4/1, 4/3, 5-11, and 12/11 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The reasons for allowance: the applied references fail to teach and/or suggest the following:

a) wherein the circuit substrate comprises a piuraiity of substrate pads which are formed on the internal surfaces of the above three areas and electrically connected to the semiconductor chips as claimed in claim 2. Note that claim 7 and 9 depend on claim 2, and claims 8 and 10 depend on claims 7 and 9.

b) the applied references fail to teach having a third semiconductor chip on the third area, and wherein the first and third chips have an identical size as claimed in claims 4 and 6.

c) wherein a rear surface of the first semiconductor chip is faced to a rear surface of the third semiconductor chip as claimed I claim 5.

d) wherein the circuit substrate comprises a plurality notches which are formed in the external surfaces of first, second and third areas at the boundaries of these three areas as claimed in claim 11.

4. Larson (US 2003/006261 A1), Kim et al. (US 6,699,730 B2), and Hashimoto (US 6,486,544 B1) shows a structure of a semiconductor device comprising a substrate having first, second and third areas; and at least two semiconductor chips are positioned within an internal space.

Telephone Inquiry Contacts

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jasmine J. Clark whose telephone number is (571) 272-1726. The examiner can normally be reached on Flex.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571) 272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jjbc/05/13/05

JASMINE CLARK
PRIMARY EXAMINER